REMARKS

By this Amendment, dependent claim 4 has been rewritten in independent form so as to include all of the features of base claim 1; claims 1, 5, 6 and 15-22 have been canceled; and minor changes have been made to claims 8-12. Accordingly, claims 4 and 7-14 are all the claims currently pending in the application.

Applicant notes that the above-noted amendments do not raise new issues that would require further consideration and/or search, and therefore, Applicant respectfully submits that the present amendment should be entered.

I. Claim Objections

Claims 5 and 8-12 were objected to due to minor informalities.

Regarding clam 5, as noted above, this claim has been canceled by the present amendment. Regarding claims 8-12, Applicant notes that each of these claims has been amended as suggested by the Examiner. In particular, in claim 8, line 2, --the-- has been added before "reconfiguration"; in claim 9, line 4, "a" was changed to --the--; in claim 10, line 2, "a" was changed to --the--; in claim 11, line 5, "a" was changed to --the--; and in claim 12, line 3, --the-- was added before "order".

In view of the foregoing, Applicant kindly requests that the claim objections be reconsidered and withdrawn.

II. Claim Rejections under 35 U.S.C. § 102

Claims 1, 4-10 and 15 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yokozeki et al. (U.S. 7,080,270, hereinafter "Yokozeki").

As noted above, claim 4 has been rewritten in independent form so as to include all of the features of claim 1. Thus, claim 4 recites the feature of a logic circuit having a configuration that can be changed in accordance with the data held in said latch circuit. Applicant respectfully submits that Yokozeki does not disclose or suggest at least this feature of claim 4.

Regarding Yokozeki, Applicant notes that this reference discloses the use of a combinational logic circuit 1, in which data that is held in a latch circuit is output to and processed by the combination logic circuit 1. In the Office Action, the Examiner has taken the position that the combinational logic circuit 1 of Yokozeki changes state based on the output of latch circuit 14 (see Office Action at page 3). Applicant respectfully disagrees.

In particular, with respect to the combinational logic circuit 1 of Yokozeki, Applicant notes that a combinational logic circuit is a logical circuit which is configured of only gate elements such as AND, OR, NOT, NAND, NOR, and exclusiveOR, and which does not include an internal memory element such as a flip-flop.

Thus, as a combinational logic circuit is known in the art to include only the above-noted gate elements, Applicant respectfully submits that while the output of the combinational logic circuit 1 of Yokozeki will change based on the data input thereto, that it is incorrect to indicate that the state of the combinational logic circuit 1 itself will undergo any change.

In this regard, Applicant notes that Yokozeki does not include any disclosure even remotely suggesting that the configuration of the combinational logic circuit 1 undergoes a change based on data held in the latch circuit.

In view of the foregoing, Applicant respectfully submits that Yokozeki does not disclose, suggest or otherwise render obvious at least the above-noted feature recited in claim

4 of a logic circuit having a configuration that can be changed in accordance with the data held in the latch circuit. Accordingly, Applicant submits that claim 4 is patentable over Yokozeki, an indication of which is kindly requested.

Claims 7-10 depend from claim 4 and are therefore considered patentable at least by virtue of their dependency. Regarding claims 1, 5, 6 and 15, as noted above, these claims have been canceled by the present amendment.

III. Claim Rejections under 35 U.S.C. § 103(a)

Claims 1, 4-10 and 15 were rejected as being unpatentable over Toyoda et al. (U.S. 6,845,032, hereinafter "Toyoda") in view of Miwa (U.S. 6,285,575, hereinafter "Miwa").

Claim 4 recites the feature of a ferroelectric capacitor circuit that includes a first circuit having a nonvolatile ferroelectric element for holding data and a second circuit having a nonvolatile ferroelectric element for holding data, wherein a switch circuit is operable to select one of the first circuit and the second circuit, and connect the selected circuit with a latch circuit only when data is transferred between the latch circuit and the ferroelectric capacitor circuit.

In the Office Action, the Examiner has relied on the Miwa reference for the teaching of a memory cell which includes a flip-flop 3, transistors M2 and M3, and a ferroelectric capacitor circuit consisting of capacitors F0 and F1 (see Fig. 7). As explained in Miwa, gate electrodes of the transistors M2 and M3 are connected to a common control line CL, wherein the control line CL becomes HIGH level during a storing operation and a recalling operation, in which the ferroelectric capacitors F0 and F1 and the flip-flop 3 are electrically connected (see col. 1, lines 57-62 and col. 2, lines 46-48). Conversely, when the control line CL of

Miwa is held LOW level, the flip-flop 3 is electrically disconnected from the ferroelectric capacitors F0 and F1 (see col. 1, lines 62-65).

Thus, while Miwa discloses the ability to connect/disconnect the flip-flop 3 from the ferroelectric circuit consisting of capacitors F0 and F1, Applicant notes that Miwa does not disclose or suggest the above-noted features recited in claim 4 of a ferroelectric circuit which includes a first circuit having a nonvolatile ferroelectric element for holding data and a second circuit having a nonvolatile ferroelectric element for holding data, wherein a switch circuit is operable to select one of the first circuit and the second circuit.

In this regard, Applicant notes that the Examiner has recognized that Miwa does not disclose or suggest such features, but nonetheless, has merely stated in a conclusory manner that "it would have been obvious to connect two additional ferroelectric capacitors to Miwa's flip-flop 3" (see Office Action at page 4). Applicant respectfully disagrees.

Initially, Applicant notes that the Examiner has provided absolutely no reasoning as to why one of ordinary skill in the art would modify Miwa in such a manner, and as such, Applicant submits that the Examiner's rejection is clearly improper. Moreover, Applicant respectfully submits that one of ordinary skill in the art would not have had any reason whatsoever to modify the circuit shown in Fig. 7 of Miwa as suggested by the Examiner.

If the Examiner disagrees, and believes that there is a rational underpinning as to why one of ordinary skill in the art would have modified Miwa in such a manner, Applicant requests that the Examiner articulate such a reasoning so that Applicant may make an informed decision with regard to appeal.

Furthermore, Applicant notes that even if two additional ferroelectric capacitors were connected to the flip-flop 3 of Miwa, as suggested by the Examiner, that the transistors M2

and M3 of Miwa would not be able to select two of the four ferroelectric capacitors, but instead, would only be able to function so as to make the entire control line CL be HIGH level or LOW level.

As such, even if one of ordinary skill in the art would somehow have been motivated to add two additional ferroelectric capacitors to the flip-flop 3 of Miwa (as noted above, Applicant disagrees with such a position), Applicant respectfully submits that the resulting circuit still would not teach or suggest the above-noted feature recited in claim 4 of a ferroelectric capacitor circuit which includes a first circuit having a nonvolatile ferroelectric element for holding data and a second circuit having a nonvolatile ferroelectric element for holding data, wherein a switch circuit is operable to select one of the first circuit and the second circuit.

In view of the foregoing, Applicant respectfully submits that the combination of Toyoda and Miwa does not teach, suggest or otherwise render obvious at least the above-noted features recited in claim 4. Accordingly, Applicant submits that claim 4 is patentable over the cited prior art, an indication of which is kindly requested.

Claims 7-10 depend from claim 4 and are therefore considered patentable at least by virtue of their dependency. Regarding claims 1, 5, 6 and 15, as noted above, these claims have been canceled by the present amendment.

IV. Allowable Subject Matter

Applicant acknowledges that the Examiner has indicated that claims 11-14 contain allowable subject matter and would be allowable if rewritten in independent form.

V. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance, an indication of which is kindly requested. If there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is kindly requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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